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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,831	06/26/2003	Mark Andrew Bickerstaff	LUTZ 2 00423	7595

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,831	BICKERSTAFF, MARK ANDREW	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Amended Claims 1-15 have been submitted for examination
- Amended Claims 1-15 have been rejected

Response to Arguments

1. Applicant's arguments see page 10, filed 3/16/2006 with respect to rejection of claim 6 under 35 USC § 112, 2nd paragraph have been fully considered but they are not persuasive. The examiner notes that the claim language clearly states "**the first trellis** is a **N1-state** Radix-K trellis and **the second trellis** is a **N2-state** Radix-K trellis". As per the applicant argument N1 and N2 have different names that are independent of each other, If N1 and N2 are related that is the only time additional condition should be added. In view of the above arguments the Examiner maintains the above rejection.

2. Applicant's arguments, see pages 9-15, filed 3/16/2006, with respect to the rejection(s) of claim(s) 1-14 under 35 USC § 102 (e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bickerstaff et al. A Unified Turbo/Viterbi Channel Decoder for 3 GPP Mobile wireless in 0.18-um CMOS, IEEE Journal of Solid-State Circuits, vol. 37, no.11, November 2002, pages 1555-1564 (Hereinafter Bickerstaff02). Copy is provided.

Information Disclosure Statement (IDS)

3. US patent application no. 2002/0162074, now patent no. 7,020,214 has been considered in the Notice of References.

Specification Objection

4. In view of the amended claim 1, line 4 and claim 10, line 2 and for consistency throughout the specifications.

The disclosure is objected to because of the following informalities:

The "**in line**" should be changed to "**in-place**" in page 8, line 24, page 13, line 30 and page 18, lines 1, 12 and 17.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-15 are rejected under 35 U.S.C. 102(a) as being anticipated by Bickerstaff02.

6. In regard to claim 1, Bickerstaff02 teaches:

- A decoder comprising:
- an SISO device that operates as a PCCC decoder in a first mode of operation and as an SCCC decoder in a second mode of operation where the device operates as per at least one trellis using an in-place addressing technique to process information.

(Note: Section B. Turbo mode, page 1557, lines (40-51) and Section A. Viterbi mode, page 1557, line 3 in Bickerstaff02)

7. In regard to claim 2, Bickerstaff02 teaches:

- The encoder of claim 1 where the device processes information in accordance with an algorithm.

(Note: Page 1555, line 29 in Bickerstaff02)

8. In regard to claim 3, Bickerstaff02 teaches:

- The encoder of claim 2 where the algorithm is a Log MAP algorithm and the SISO device is a Log MAP processor.

(Note: Page 1555, line 29 in Bickerstaff02)

9. In regard to claim 4, Bickerstaff02 teaches:

- The encoder of claim 1 where in the first mode of operation the SISO device operates as a first SISO during one time period and in the second mode of operation operates as a second SISO device during a second time period where the first and second SISO devices process information as per the same or different trellis.

(Note: Page 1557, lines (35-38) in Bickerstaff02)

10. In regard to claim 5, Bickerstaff02 teaches:

- The encoder of claim 1 where in second mode of operation the SISO device operates as an inner SISO during one time period whereby it processes information as per a first trellis and operates as an outer

SISO during another time period whereby it processes information as per a second trellis.

(Note: Page 1557, lines (35-38) in Bickerstaff02)

11. In regard to claim 6, Bickerstaff02 teaches:

- The encoder of claim 5 where the first trellis is a N1-state Radix-K trellis and the second trellis is a N2-state Radix-K trellis where N1 may or may not be equal to N2 and K, N1 and N2 are integers equal to 1 or greater.

(Note: Abstract in Bickerstaff02)

11. In regard to claim 7, Bickerstaff02 teaches:

- The encoder of claim 1 where the SISO device comprises:
- at least one branch metric calculator',
- at least one forward path metric calculator and at least one backward path metric calculator where both calculators are in communication with the branch metric calculator;
- at least one Log Likelihood calculator coupled to the path metric calculators; and
- at least one subtractor circuit having an extrinsic information input and coupled to the at least one Log Likelihood calculator to provide at least one Log Likelihood ratio output whereby the path metric calculators and the at least one Log Likelihood calculator are constructed with Log

Sum operators which are designed based on an approximation of a Jacobian definition of a Log Sum operation.

(Note: any of figures 4, 5 or 7 in Bickerstaff02)

12. In regard to claim 8, Bickerstaff02 teaches:

- The encoder of claim 7 in which the information is processed as per an N1 state Radix-K first trellis and an N2 state Radix-K second trellis when operating as an SCCC turbo decoder where N1 is not equal to N2 and where N1 and N2 are integers equal to 2 or greater and K is an integer equal to 4 or greater.

(Note: Section C A turbo Decoding, page 1556 in Bickerstaff02)

13. In regard to claim 9, Bickerstaff02 teaches:

- The encoder of claim 7 where the SISO device is operating as a PCCC decoder and N1 is equal to N2 and K is an integer equal to 4 or greater and N1; N2 are integers equal to 2 or greater.

(Note: Section C A turbo Decoding, page 1556 in Bickerstaff02)

14. In regard to claim 10, the Applicant Admitted Prior Art (Hereinafter AAPA) teaches:

- The encoder of claim 1 where the A in-place addressing technique uses a block of memory for retrieving and storing values of the states of the trellis as the device processes the received information.

(Note: page 8, lines (6-14) in AAPA specifications)

15. In regard to claim 11, AAPA teaches:

- The encoder of claim 1 where information is processed using a portion of the states of the trellis to perform the in-place addressing technique during a clock cycle.

(Note: page 8, lines (6-14) in AAPA specifications)

16. In regard to 12, Bickerstaff02 teaches:

- A method of performing turbo decoding, the method comprising the step of:
- processing, in accordance with an algorithm, received information as per an N-state Radix-K trellis using an in-place addressing technique where N, K are integers equal to 1 or greater.

(Note: section B. Turbo decoding, page 1557 in Bickerstaff02)

17. In regard to claim 13, Bickerstaff02 teaches:

- The method of claim 12 where the received information is processed as per an N-state Radix-K trellis using an in-place addressing technique where N is an integer equal to 2 or greater and K is an integer equal to 4 or greater.

(Note: section B. Turbo decoding, page 1557, lines (29-34) in Bickerstaff02)

18. Claim 14 is rejected for the same reasons as per claim 13.

19. In regard to claim 15, Bickerstaff02 teaches:

- A decoder comprising:
- an interleaver;
- a deinterleaver; and

- a soft input soft output device in communication with the interleaver and the deinterleaver the soft input output device being operative to use an in-place addressing techniques when processing path metric data related to each of the states of a trellis , whereby a block of memory storing the path metric data is sequentially processed in a plurality of equally sized groups in accord with a trellis processing algorithm , and whereby when data from a selected one of the groups is read from an associated group of memory locations in a current pass of the trellis processing algorithm, those memory locations are made available to receive and store output data from the trellis processing algorithm, and whereby output data from the trellis processing algorithm that is appropriately stored in memory locations of the selected group is stored in memory locations of the selected group and output data that is appropriately stored in a memory location of a second group, from which data has not been yet been read in the current pass of the trellis processing algorithm, the output data that is appropriately stored in a memory location of the second group is stored in a hold register and whereby when data from the second group is read from the associated second group of memory locations, those memory locations are made available to receive and store output data from the trellis processing algorithm and appropriate data from the hold register is copied into the newly available appropriate memory

locations associated with the second group, whereby the same block of memory is used to store input data to the trellis processing algorithm and output data from the trellis processing algorithm and whereby an order of the plurality of groups of data may be rearranged within the block of memory, thereby facilitating the further processing of the data according to M butterfly mapping and thereby allowing the decoder to be used to process a trellis of arbitrary size.

(Note: Fig. 4 (Extrinsic/ Path History Memory), (input Buffer) and (s Table) references in Bickerstaff02)

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Allan, Gord A 2.5 mW – 10 Mbps, Low Area MAP Decoder Pages 1-25, May 7, 2002. Note page 23 of 25, reference [11]

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

5/12/06

GUY LAMARRE
PRIMARY EXAMINER